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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,151	09/25/2003	William E. Wall	A-8839	4560

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EXAMINER	
LUONG, ALAN H	
ART UNIT	PAPER NUMBER
2427	

NOTIFICATION DATE	DELIVERY MODE
10/29/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOmail@sciatl.com

Office Action Summary	Application No.	Applicant(s)	
	10/671,151	WALL ET AL.	
	Examiner	Art Unit	
	ALAN LUONG	2427	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Art unit is changed into 2427.

2. Claims 1-3, 5-6 and 8 have been amended. Therefore, claims 1-6 and 8 are pending in this application.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on Sept 09, 2008, has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1- 6 and 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,184,664 issued to Farmer et al. (Hereinafter Farmer); in view of US Pub. 2002/0063924 by Kimbrough et al (Hereinafter Kimbrough).

Regarding to claim 1: Farmer discloses a fiber-to-the-home (FTTH) system (col. 1 lines 22-25), comprising:

Fig. 1 illustrates [117] is "at least one **digital home communications terminal (DHCT)"** for "**receiving forward signals from a headend facility**" [110] and for "**transmitting reverse RF signals**" back to "the **headend facility**" (see **Farmer col. 7, lines 40-59)**; referring to Fig. 3, showing the headend facility [110] can further comprise a logic interface [350] is connected to a laser transceiver node routing device [355], the reverse RF signals, optical RF packets are fed into an optical receiver [370] where the upstream optical RF packets are converted from the optical domain into the electrical domain, are then fed into [355] wherein associates with [350], can read **packet headers** originating from the nodes [120] and the internet router [340]. The logic interface [350] can also translate interfaces with the telephone switch [345]. After reading the **packet headers**, the logic interface 350 and laser transceiver node routing device 355 can determine where to send the packets of information".(**Farmer col. 12, lines 45-53 and lines 28-35)** meets the limitation of regarding "**the reverse RF signals including header information and payload data";**

Fig. 1, 2, 8 and 9 show "**a single wire return device** (SWRD)" [140] for "**receiving the reverse RF signals**" from the at least one **DHCT** [117] (see **Farmer col. 8, lines 1-9, Fig. 8, col. 20 lines 4-49 and Fig. 9 col. 22 lines 49-56)**, and Fig. 10 a-10c illustrates **an upstream demodulator** including RF diplexer [507], LO [531], RF detector [517] and downconverter [527], RF signals are supplied from the video service terminal 117 to RF diplexer 507, which separates the higher-frequency downstream RF signals from the

lower-frequency upstream signals, is mixed with LO [531], data outputs from mixer is detected by [517] and is converted by A/D [509] before downconverting at [527] for "**demodulating the reverse RF signals**"(see **Farmer col. 23, line 49 to col. 25 line 29)**,, and microprocessor [550] connected with Data interface [555] by selecting switch [513] for "**converting the demodulated signals**" from [407] "**to Ethernet signals**" at [555], (**Farmer col. 21, lines 4-9)**;

an optical network terminal (ONT) includes [515], [525], [520], [530] and [540] which are **coupled to the SWRD,** RF packets as the Ethernet signals are inputted in Optical transmitter [530] **"for converting the Ethemet signals"** to 1310nm **"optical signals"** and for **"transmitting the optical signals to the headend facility** [110] **via optical fiber** [150] **(Farmer col. 21, lines 43-52 and Fig. 18, col. 36, line 45- col. 37 line 22)**; and Fig. 3 depicts **a plurality of downstream modulators** [310], [315] located in **the headend facility** [110] remote from the upstream demodulator **(Farmer col. 10, lines 59-67)**

However, Farmer fails to disclose "with each downstream modulator associated with at least one corresponding DHCT and having an identification number that is inserted into the forward signals from the headend facility to identify that downstream modulator to the at least one corresponding DHCT, one of said downstream modulators associated with the at least one DHCT for receiving the optical signals and for sending the forward signals;

In an analogous art directed toward a similar problem namely improving the results from downstream modulator having an identification number. Fig. 8 of Kimbrough illustrates a Quad Optical Interface Unit [20A] as "**a downstream modulator associated with at least one corresponding DHCT"** as HNU [50] and QOIU 20A has an Ethernet MAC address as **an identification number.** Since both voice and data are packetized in this system, the QOIU 20A needs to know the various MAC (Media Access Control) addresses of the HNUs 50 to enable proper packet delivery down the fiber network, it is obvious the Ethernet MAC address of QOIU 20A to be **inserted into the forward signals from the headend facility** [12] **to identify that downstream modulator** [QOIU 20A] **to the at least one corresponding DHCT** [50], When a particular HNU 50 is attached to the system, the HNU 50 starts sending packets, which are typically voice packets, upstream towards the Quad OIU 20A (with identified address of Quad OIU 20A) with the HNU's source MAC address embedded in these packets. The packets from the particular HNU 50 are routed into the common FPGA 134 and stored in the SRAM 138. Each time the common FPGA 134 detects a new HNU 50, it interrupts the RISC processor 136, and the processor 136 goes out and learns the MAC address of the new HNU 50 so that the QOIU 20A knows how to properly address downstream packets to that HNU 50." (Kimbrough, ¶0105, ¶0108) meets the limitation of **"one of said downstream modulators associated with the at least one DHCT for receiving the optical signals and for sending the forward signals";**

Fig. 9 illustrates HNU [50] **wherein the at least one DHCT** [52] includes processor [158] is coupled to the control FPGA 150, and stores the MAC address for the HNU 50 and also handles the learning of the Quad OIU card 20A address so that the HNU 50 addresses its voice packets correctly by **"inserting the modulator identification number"** as the Quad OIU card 20A address, **received within the forward signals from the headend facility** [12] **into the reverse header information** of reverse signal (Kimbrough, ¶0114, ¶0109 and ¶0112), and the control FPGA [150] **wherein the SWRD** [50], also drives the 10Base-T Ethernet PHY 54, which is an integrated circuit converts **the modulator identification number within the reverse header information** as the physical layer transport of Ethernet packets as **an Internet Protocol address number** to and from the subscriber's data network or **enable the reverse signals to be directed to said one downstream modulator.** (Kimbrough, ¶0116). Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to modify a RF return system of Farmer with a downstream modulator as taught by Kimbrough, in order to provide a multi-media access system that is scalable and which does not include complex, costly intermediate electronics in the local access loop between the central office location and the subscriber's premises. (Kimbrough, ¶0010).

Regarding to claim 2: Farmer discloses the FTTH system of claim 1 above, with the SWRD comprising:

block 507 of Fig. 8 is **a diplex filter** coupled for filtering forward signals and the reverse RF signals; (Farmer, col. 23 lines 1-3, lines 53-56)

Fig. 10 a-10c illustrates **an upstream demodulator** including RF diplexer [507],

LO [531], RF detector [517] and downconverter [527], coupled to the diplex filter for demodulating the reverse RF signals;(**Farmer col. 23, line 49 to col. 25 line 29)**)

block 550 of Fig. 8 is **a microprocessor** [550] connected with Data interface [555] by selecting switch [513] for "**converting the demodulated signals**" from [407] "**to Ethernet signals**" at [555], (**Farmer col. 21, lines 4-9)**; and

Block 513 of Fig. 8 is **a switch for receiving the Ethernet signals** from [407] send to Optical Transmitter [530] for upstream signal **and any additional signals from a second source** [555] when connecting to processor [550], **the switch for combining the signals and for providing a combined signal to the ONT**.(**Farmer, col. 3, lines 29-34 and col. 21 line 43-52).**

Regarding to claim 3: The FTTH system of claim 2, Fig. 8 of Farmer shows [550] is a micprocessor **wherein the receiving device** [140]includes Digital Optical receiver [540] converts the Optical data signal into Electrical Data signal, feeds into [550] where **converts the identification number into the Internet Protocol address via the microprocessor** [550]. (Farmer, col. 21, lines 4-19).

Additional rejection for claim 3, Kimbrough also teaches the control FPGA [150] **wherein the SWRD** [50], also drives the 10Base-T Ethernet PHY 54, which is an integrated circuit converts **the modulator identification number within the reverse header information** as the physical layer transport of Ethernet packets as **an Internet Protocol address number** to and from the subscriber's data network or **enable the**

reverse signals to be directed to said one downstream modulator. (Kimbrough, ¶0116).

Regarding to claim 4: the FTTH system of claim 1, Farmer discloses wherein "the **ONT** includes block [515, 520, 530, 540 and 525] **receives the forward signals** as 1550nm optical signal via waveguide [160], [170], **wherein the forward signals comprise at least one of a telephone signal, Ethernet signals, data signals** via waveguide [170] at port [365] (Farmer, Fig. 3, col.11 line 65 to col.12 line 56)**, and audio/video signals** via waveguide [160] at port [335], (Fig. 3, col.11 lines 38-52) and Fig. 8 illustrates Digital Optical receiver [540] as a component of **the ONT wherein** receives the forward Optical signal from [150], converts optical signals into electrical binary/digital signals so that the electrical data signals can be handled by processor 550 wherein **provides the at least one of Ethernet signals** at [555] (Fig. 8, col. 20 lines 22-29 and col. 21 lines 4-19) **and provides the telephone signals to a connected telephone** [560] (col. 21 lines 9-19) **, and** the Analog optical receiver [525] can convert the downstream broadcast optical video signals into modulated **audio/video signals** and downstream **data signals** control signals into analog RF signals that are propagated through **to** an RF diplexer [507] **of the SWRD [140]** and out of the modulated RF signal input/output 535.**audio/video signals** (Fig. 8, col. 20 lines 38-49) **and provides the telephone signals to a connected telephone.** (**col.17, lines 39-54 and Fig. 7 block 555, 560 and 550**).

Regarding to claim 5: With respect to "a method for transmitting reverse signals in a fiber-to-the-home (FTTH) network, the FTTH network including a forward path and a reverse path", claim 5 merely repeats the same features of claim 1, so it is anticipated by Farmer, Kimbrough (see claim 1 rejection)

Regarding to claim 6: The method of claim 5,-merely repeats the same a portion feature of claim 1 which is rejected by Kimbrough reference, claim 6 is anticipated by Farmer and Kimbrough, (see claim 1 rejection) .

Regarding to claim 8. The method of claim 5, merely repeats the same features of claim 4, claim 8 is anticipated by Farmer and Kimbrough, (see claim 4 rejection).

Response to Arguments

Applicant's arguments with respect to claims 1-6 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALAN LUONG whose telephone number is (571)270-5091. The examiner can normally be reached on Mon.-Thurs., 8:00am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Beliveau can be reached on (571) 272-7343. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. L. /
Examiner, Art Unit 2427

/Scott Beliveau/
Supervisory Patent Examiner, Art Unit 2427